Amendments to the Claims:

Please amend claims 1, 10, 11, 14-16, 18, 22 and 23 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit chip arrangement comprising:

an integrated circuit chip having circuitry therein including a plurality of magnetically-responsive nodes adapted to store bits;

a package having magnetic material and covering at least a portion of circuitry in the integrated circuit chip; and

a sense circuit adapted to store selected bits of the plurality of magnetically-responsive nodes, the bits defining a value as a function of the magnetic material in the package,~~package; and~~

wherein the package and the plurality of magnetically-responsive nodes being arranged such that altering the package results in a state change of at least one of the plurality of magnetically-responsive nodes, the state change being detectable by the sense circuit.

2. (previously presented) The integrated circuit chip arrangement of claim 1, further comprising: an enable register adapted to store selected bits of the plurality of magnetically-responsive nodes, the value of the bits being responsive to the magnetic material in the package.

3. (previously presented) The integrated circuit chip arrangement of claim 2, wherein a cryptographic key is formed from the bits having data stored in the enable register.

4. (original) The integrated circuit chip arrangement of claim 3, wherein the integrated circuit chip arrangement is adapted for encrypting data as a function of the cryptographic

key generated using the bits having data stored in the enable register.

5. (original) The integrated circuit chip arrangement of claim 2, further comprising: a power-up state machine coupled to the enable register and coupled to the sense circuit.

6. (original) The integrated circuit chip arrangement of claim 2, wherein the selected magnetically stored bits are read to decrypt encrypted data.

7. (original) The integrated circuit chip arrangement of claim 2, wherein the integrated circuit chip is further adapted to mask an output read from the magnetically-responsive nodes using the data stored in the enable register and to store the masked output in an output register, the contents of the output register being used for encrypting data.

8. (original) The integrated circuit chip arrangement of claim 7, wherein the contents of the output register are used for decrypting data.

9. (original) The integrated circuit chip arrangement of claim 8, wherein the output register is configured and arranged to erase data stored therein upon power loss, and wherein the enable register is adapted to mask an output read from the magnetically-responsive nodes and stored in the output register upon restoring power to the output register.

10. (currently amended) An integrated circuit chip arrangement comprising:

an integrated circuit chip having circuitry therein including a plurality of magnetically-responsive nodes adapted to store bits;

a package having magnetic material and covering at least a portion of circuitry in the integrated circuit chip; and

a cryptographic circuit adapted to store selected bits of the plurality of magnetically-responsive nodes in an enable register, the value of the bits being responsive to the magnetic material in the package,~~package;~~

wherein the integrated circuit chip being adapted for encrypting data as a function of cryptographic key data in the enable register; and the package and the plurality of magnetically-responsive nodes being arranged such that removing a portion of the package alters at least one bit of the plurality of magnetically-responsive nodes having a bit stored in the enable register.

11. (currently amended) The integrated circuit chip arrangement of claim 10~~, wherein the~~ further comprising a sense circuit ~~is further~~ adapted for encrypting data as a function of the selected bits of the plurality of magnetically-responsive nodes.

12. (original) The integrated circuit chip arrangement of claim 10, wherein the integrated circuit chip is further adapted for reading (decrypting) data as a function of the selected bits of the plurality of magnetically-responsive nodes.

13. (original) The integrated circuit chip arrangement of claim 12, wherein the integrated circuit chip is further adapted to mask an output read from the magnetically-responsive nodes using the data stored in the enable register and to store the masked output in an output register, the contents of the output register being used for reading the data.

14. (currently amended) The integrated circuit chip arrangement of claim ~~12~~ 13, wherein in response to the at least one bit of the plurality of magnetically-responsive nodes being altered, the data stored in the output register is different than the data stored in the enable register.

15. (currently amended) The integrated circuit chip arrangement of claim 14, wherein the enable register is adapted to mask ~~the~~ data read from the plurality of magnetically-responsive circuit nodes with ~~the~~ data stored in the enable register such that only bits from the magnetically-responsive circuit nodes having a corresponding bit in the enable register are stored in the output register.

16. (currently amended) An integrated circuit chip arrangement comprising:

an integrated circuit chip having circuitry therein including a plurality of magnetically-responsive nodes adapted to store bits;

a package having magnetic material and covering at least a portion of circuitry in the integrated circuit chip;

a sense circuit adapted to store selected bits of the plurality of magnetically-responsive nodes, the bits defining a value as a function of the magnetic material in the package; the package and the plurality of magnetically-responsive nodes being arranged such that altering the package results in a state change of at least one of the plurality of magnetically-responsive nodes, the state change being detectable by the sense circuit, ~~circuit,~~ and

a power-up responsive circuit adapted to read data from the plurality of magnetically-responsive nodes.

17. (original) The integrated circuit chip arrangement of claim 16, further including an enable register and wherein the power-up responsive circuit is adapted to access the enable register as a function of the data from the plurality of magnetically-responsive nodes.

18. (currently amended) A method for protecting data in an integrated circuit chip having magnetically-responsive nodes adapted to store data as a function of a magnetic state, the method comprising:

packaging the integrated circuit chip using a packaging material having magnetic material, the magnetic material being arranged to set a magnetic state of a plurality of the magnetically-responsive nodes; and

using an output from the plurality of magnetically-responsive nodes to decrypt data stored in the integrated circuit chip.

19. (original) The method of claim 18, further comprising: storing an address location of selected ones of the plurality of magnetically-responsive nodes in an enable register; and wherein using an output from the plurality of magnetically-responsive nodes to decrypt

data stored in the integrated circuit chip includes using the address information stored in the enable register to mask an output read from the plurality of magnetically-responsive nodes and storing the masked output in a key register and using the key register to decrypt data.

20. (original) The method of claim 19, further comprising encrypting data using bits from the selected ones of the plurality of magnetically-responsive nodes having their address location stored in the enable register.

21. (original) The method of claim 19, wherein storing an address location of selected ones of the plurality of magnetically-responsive nodes in an enable register includes: testing the plurality of magnetically-responsive nodes for stability; and selecting stable ones of the plurality of magnetically-responsive nodes and storing address information for the stable ones of the magnetically-responsive nodes in the enable register.

22. (currently amended) The method of claim 21, further comprising: testing stable ones of the magnetically-responsive nodes for randomness; and wherein storing address information for the stable ones of the magnetically-responsive nodes in the enable register includes storing address information for selected ones of the magnetically-responsive nodes exhibiting ~~a selected degree of~~ randomness.

23. (currently amended) The method of claim 22, wherein storing an address location of selected ones of the plurality of magnetically-responsive nodes in an enable register includes storing a data "one" in the enable register for each of the selected ones of the plurality of magnetically-responsive nodes and wherein storing address information for selected ones of the magnetically-responsive nodes exhibiting a selected degree of randomness includes setting a value for selected ones of the magnetically-responsive nodes not exhibiting ~~a selected degree of~~ randomness to a data "zero."

24. (original) The method of claim 18, prior to packaging the integrated circuit chip, further comprising: selecting a characteristic of magnetic particles in a package to

maximize stability of the state of the plurality of magnetically-responsive nodes; and wherein packaging the integrated circuit chip includes arranging the magnetic material in response to the selected characteristic.

25. (original) The method of claim 24, wherein selecting a characteristic of magnetic particles includes selecting at least one of: size and strength characteristics of the magnetic particles.